

WHAT IS CLAIMED IS:

1. A contact hole formation method for forming contact holes in an area in which gate electrodes are densely formed and an area in which gate electrodes are sparsely formed, comprising:
 - a process of depositing a first dielectric film on a semiconductor substrate on which transistors are formed;
 - a process of planarizing the first dielectric film;
 - a process of depositing, on the first dielectric film, a second dielectric film having an etching rate different from an etching rate of the first dielectric film; and
 - a process of forming the contact holes through the first and second dielectric films.
2. The contact hole formation method according to claim 1, further comprising a process of planarizing the second dielectric film.
3. The contact hole formation method according to claim 1, wherein the first dielectric film is a BPSG film.
4. The contact hole formation method according to claim 3, wherein, after planarization of the first dielectric film, the second dielectric film is deposited on the first dielectric film before a precipitate is formed on a surface of the first dielectric

film.

5. The contact hole formation method according to claim 4, wherein the second dielectric film is deposited on the first dielectric film within 24 hours after planarization of the first dielectric film.

6. The contact hole formation method according to claim 1, further comprising a process of eliminating a precipitate on a surface of the first dielectric film after planarization of the first dielectric film.

7. The contact hole formation method according to claim 1, wherein the contact holes are formed so as to reach the semiconductor substrate.

8. The contact hole formation method according to claim 1, wherein the contact holes are formed so as to reach the gate electrode formed on the semiconductor substrate.

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9. A contact hole formation method for forming contact holes in a semiconductor device having an area in which interconnections are densely formed and an area in which interconnections are sparsely formed, comprising:

25 a process of depositing a first dielectric film on a

semiconductor substrate on which the interconnections are formed;
a process of planarizing the first dielectric film;
a process of depositing, on the first dielectric film,
a second dielectric film having an etching rate different from
5 an etching rate of the first dielectric film; and
a process of forming the contact holes through the first
and second dielectric films.

10. A contact hole formation method for forming contact
10 holes in a semiconductor device having a semiconductor substrate
on which a plurality of interconnections of different widths are
formed, comprising:

a process of depositing a first dielectric film on the
semiconductor substrate on which the interconnections are formed;
15 a process of planarizing the first dielectric film;
a process of depositing, on the first dielectric film,
a second dielectric film having an etching rate different from
an etching rate of the first dielectric film; and
a process of forming the contact holes through the first
20 and second dielectric films.

11. A semiconductor device, comprising:
a substrate having an area in which gate electrodes are
densely formed and an area in which gate electrodes are sparsely
25 formed;

a first dielectric film formed on the substrate and provided with a planarized surface; and

a second dielectric film formed on the planarized surface of the first dielectric film and provided with an etching rate
5 different from an etching rate of the first dielectric film, and

wherein contact holes are formed through the first and second dielectric films.

12. The semiconductor device according to claim 11,
10 wherein the second dielectric film is planarized.

13. A semiconductor device, comprising:

a substrate having an area in which interconnections are densely formed and an area in which interconnections are
15 sparsely formed;

a first dielectric film formed on the substrate and provided with a planarized surface; and

a second dielectric film formed on the planarized surface of the first dielectric film and provided with an etching rate
20 different from an etching rate of the first dielectric film, and

wherein contact holes are formed through the first and second dielectric films.

14. A semiconductor device, comprising:

25 a substrate on which a plurality of interconnections

on different widths are formed;

a first dielectric film formed on the substrate and provided with a planarized surface; and

5 a second dielectric film formed on the planarized surface of the first dielectric film and provided with an etching rate different from an etching rate of the first dielectric film, and

wherein contact holes are formed through the first and second dielectric films.

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